5.5: Transient and Steady-State Improvement

Lead–Lag and PID Designs

When control system design specifications require simultaneous improvement to the transient response and the steady-state tracking error, a lead-lag or a PID controller may be considered. A lead-lag controller combines phase-lead and phase-lag stages; a PID controller similarly combines PD and PI controllers. In the two-stage design, the transient response is improved first, followed by steady-state error improvement. The design steps are illustrated in the following example.

Example \(\PageIndex{1}\): Lead-Lag Design

Let \(G(s) = \frac{10}{s(s+2)(s+5)}\); assume that the design specifications are: \(\% OS \leq 10\%\), \(t_s \leq 2\ s\), \(e_{ss} \big|_{\text{ramp}} \leq 0.1\). These specifications translate into: \(\zeta \geq 0.6\), \(\sigma \geq 2\), \(K_v \geq 10\).

**Phase-Lead Design.** The phase-lead controller design proceeds as follows: Let \(s_1 = -2.2 \pm j2.3\); \(\zeta = 0.69\); then, \(G(s_1) = 0.38 \angle 92^\circ\), i.e., the required controller phase contribution is: \(K(s_1) = K \angle 88^\circ\).

Let \(z_c = 2\), \(p_c = 24\); then \(K(s_1) = 0.11 \angle 88^\circ\). From the RL plot, a controller gain \(K = 25\) is selected for closed-loop roots at: \(s = -2.24 \pm j2.28\). Hence, the controller is defined as: \(K(s) = 25 \left(\frac{s+2}{s+24}\right)\).

**Phase-lag Design.** For \(K_{\text{lead}}(s)G(s)\), we have \(K_v = 0.083\). To boost the error constant to \(K_v = 10\), a phase-lag controller, \(K_{\text{lag}} = \frac{s+0.05}{s+0.004}\) is considered. The angle contribution of the phase-lag controller is: \(\angle K_{\text{lag}} \big|_{\text{left}(s_1)} = -0.6^\circ\).
The lead-lag controller is formed as: \(K(s) = 25\left(\frac{s+2}{s+24}\right)\left(\frac{s+0.05}{s+0.004}\right)\).

The closed-loop transfer function is obtained as: \(T(s) = \frac{250(s+0.05)}{(s+0.051)(s+24.5)(s^2+4.43s+9.97)}\). The dominant closed-loop roots are located at: \(s = -2.22 \pm j2.25\) \(\zeta = 0.7\).

The step and ramp responses of the closed-loop system are plotted in Figure 5.9. The step response shows a settling time of \(2.5\text{sec}\), which is slightly higher than desired \(t_s = 2\text{sec}\).

Figure 5.9: Unit-step response (left) and unit-ramp response (right) of the closed-loop system (Example 5.10).

Example 5.10 (Lead-lag Design):

Example 2: PID Design

Let \(G(s) = \frac{10}{s(s+2)(s+5)}\); assume that the design specifications are: \(\%\text{ O.S.} \leq 10\%, \ t_s \leq 2\text{sec}, \ e_{\text{SS}}|_{\text{ramp}} \leq 0.1\). These specifications translate into: \(\zeta \geq 0.6, \ \sigma \geq 2, \ K \geq 10\).

**PD design.** The PD controller is given as: \(K_{PD}(s) = K(s+z_c)\). We may arbitrarily select a zero location: \(z_c = -2\), and use the root locus of the compensated system to select \(K = 1.2\) for closed-loop roots at: \(s_1 = -2.5 \pm j2.4\).

**PI design.** The PI controller is given as: \(\frac{s+z_c}{s}\), where \(z_c \ll s_1\). We may arbitrarily select a zero location: \(z_c = 0.05\) to define the PID controller as: \(K_{PID}(s) = \frac{1.2(s+0.05)(s+2)}{s}\).

The closed-loop transfer function is given as: \(T(s) = \frac{12(s+0.05)}{(s+0.051)(s+2)(s^2+4.95s+11.75)}\).

The step response of the closed-loop system shows a settling time of \(t_s = 2.3\text{sec}\) (Figure 5.9).

Alternatively, we can combine the phase-lead controller design with a PI controller to define the composite controller.

Example 3: Phase-Lead with PI

Let \(G(s) = \frac{10}{s(s+2)(s+5)}\); assume that the design specifications are: \(\%\text{ O.S.} \leq 10\%, \ t_s \leq 2\text{sec}, \ e_{\text{SS}}|_{\text{ramp}} \leq 0.1\). These specifications translate into: \(\zeta \geq 0.6, \ \sigma \geq 2, \ K \geq 10\).

**Phase-Lead Design.** Let \(s_1 = -2.2 \pm j2.3\), \(\zeta = 0.69\); then, we may choose, for example, \(z_c = 2, \ p_c = 24\) and \(K = 25\) for closed-loop roots at: \(s = -2.24 \pm j2.28\). Hence, the controller is defined as: \(K(s) = 25\left(\frac{s+2}{s+24}\right)\).

**PI design.** The PI controller is given as: \(\frac{s+z_c}{s}\), where \(z_c = 0.05\).

The composite controller is formed as: \(K(s) = 25\left(\frac{s+2}{s+24}\right)\left(\frac{s+0.05}{s}\right)\).
The resulting closed-loop transfer function is: 
\[ T(s) = \frac{250(s+0.05)}{(s+0.051)(s+24.5)(s^2+4.43s+9.95)} \],
which has dominant closed-loop roots located at: \( s = -2.21 \pm j2.25 \ (\zeta = 0.7) \).

The step response of the closed-loop system shows a settling time of \( t_s = 4.8 \text{sec} \) (Figure 5.9).

The controllers introduced in Examples 5.9 and 5.10 add a slow mode, \( (e^{-0.05t}) \), to the step response of the closed-loop system. However, the contribution of this mode to the closed-loop step response, as determined by PFE is relatively small (\( 2.5\% \)).

Figure 5.9: Root locus design of the PD controller (left); the step response of the closed-loop system for PID controller and the phase-lead with PI controllers (right).

MATLAB Tuning of PID Controller

The MATLAB Control Systems Toolbox offers the 'pidtune' command to design an optimal PID controller. The command can be used to design a regular PID controller or PID controller with filter.

Example 4: MATLAB PID Controller

Let \( G(s) = \frac{10}{s(s+2)(s+5)} \); then, the MATLAB tuned PID controller is obtained as:
\[ K(s) = \frac{2.01(s+0.314)(s+1.43)}{s} \]

The resulting closed-loop roots are located at: \( s = -0.34, -1.16, -2.73 + 3.71j \)

Alternatively, the MATLAB tuned PID controller with filter is obtained as:
\[ K(s) = \frac{727.25(s+0.302)(s+1.41)}{s(s+361.4)} \]

The resulting closed-loop roots are located at: \( s = -0.34, -1.16, -2.73 + 3.71j, -361.5 \)

The closed-loop system responses for the MATLAB designed PID controllers are plotted in Figure 5.10. The responses are almost identical and display a settling time of \( t_s \cong 6 \text{sec} \).
Figure 5.10: Unit-step response of the closed-loop system for MATLAB tuned PID controllers.