Metal Oxide Semiconductors

The metal-oxide ($\text{SiO}_2$)-semiconductor (Si) is the most common microelectronic structures nowadays. The two terminals of MOS-Capacitor consist of the main structures in MOS devices and it is the simplest structure of MOS devices. Therefore, it's essential to understand the mechanisms and characteristics of how MOS-C operates. The mechanisms under static biasing conditions can be visualized from two diagrams.

1. Energy band diagram
2. Block-charge diagram

The characteristics of MOS-C can be visualized by C-V (Capacitance verses Voltage) curves.

Introduction

The principals of forming MOS structure are similar to the metal-semiconductor (MS) contact structures, but the MOS structure is like a sandwich structure which have a thin layer of silicon oxides in the middle between metal and semiconductor (Si) layer. Figure 1 below shows a schematic of an ideal MOS-C device. For an ideal MOS-C structure, some properties should follow below.

1. The metallic gate should thick enough to be equipotential region, where every points has the same potential in the space, under a.c and d.c biasing conditions.
2. The oxides layer in the middle should be a perfect insulator with zero current flowing through under all static biasing conditions.
3. There should be no charge centers located on the oxide-semiconductor interface.
4. The semiconductor should be uniformly doped with donors or acceptors as p-type or n-type semiconductors.
5. The semiconductor (Si) should be thick enough for charges to encounter a field free region (Si bulk) before
reaching the back contact.

6. The Ohmic contacts should be established on the backside of the MOS device.

7. MOS-C is a one-dimensional structure with variables only related to the x-coordinate (distance) as the Figure 1 below.

8. The metal work function ($\Phi_M$) should equal to the semiconductor work function ($\Phi_S$) as well as the electron affinity ($\chi$) with the difference of conduction band ($E_c$) and Fermi energy ($E_F$) in forward flat band, $\Phi_M=\Phi_S=\chi+(E_c-E_F)_{FB}$. This property can be omitted, but it is easier to help with the initial understanding of the static behavior in MOS devices.

Figure 1: The schematic of an ideal MOS-C device

Energy Band and Block Charge Diagrams

The band diagram shows the band energy of the materials and how their energy levels change in the process as functions of spatial dimensions. The X-axis represents the distance (x) in the cross-section view of the MOS devices. The Y-axis represents the energy. There are no arbitrary values for Y but only relative values. As the Y-axis is increasing, the corresponding energy is higher. In the figure 2 below is the energy band diagram of MOS-C in flat band with n-type semiconductor. The $E_{vc}$ is the vacuum level which is the minimum energy an electron must reach in order to free from the material. The work function $\Phi_M$ and $\Phi_S$ are the amount of work to remove an electron, so it's the difference between Fermi level ($E_F$) and $E_{vc}$. The electron affinity ($\chi$) specifies the height of energy barrier in semiconductors, so the $\chi_i$ is the energy barrier of the insulator (oxides SiO$_2$). The zero-bias band diagram in figure 2 (a) is called flat band diagram. The formation of this band diagram can conceptually think of the equilibrium metal-semiconductor contact but is separated with a distance $x_0$, the thickness of the oxide layer. The Fermi level aligned between metal and semiconductor since it's specified in the property 8 above. Since there are no charge or electric field in the flat band MOS-C device, the inserted insulator can only have an effect in slightly lowering the energy barrier and there is no block charge diagram for flat band like figure in 2(b).
The block charge diagram shows the charge density distribution inside the MOS structure. Like the energy band diagram, the X-axis represents the distance (x) in the cross-section view. However, the Y-axis represents the exact charge distribution Q in the MOS devices. There are two horizontal Y-axis which represent the metal-oxides interface and oxide-semiconductor interfaces. The region above X-axis is the positive charge Q which is created by holes concentration, while the region below X-axis is the negative charge Q which is created by electrons concentration.

Figure 2 (a) The flat band diagram of MOS-C in equilibrium with n-type semiconductor, (b) the block charge diagrams of flat band MOS-C.

Effect of an applied bias

Other than the flat band in the MOS structure, as the d.c bias VG apply to the MOS-C devices. Three different types of biasing regions with different shape of both energy band and corresponding block charge diagram occur and they are showed in figure 3, 4, 5 and 6 below for n-type semiconductors. However, the types of biasing regions are also different from n-type and p-type semiconductor because of the different positions of the Fermi level as well as the doped charges. Since the focus is the mechanisms under biasing conditions, the p-type diagrams follow the same concepts but are not discussed here. One thing worth mentioning is that the Fermi level of semiconductor does not change when VG is applied. Therefore, the VG can be calculated as the equation (1) shown below, where q is the electric charge.
The first type of biasing region is accumulation, where the majority carrier concentration is greater near the oxide-semiconductor interface than in the bulk of the semiconductor. This happens for n-type semiconductor when $V_G > 0$. From the band diagram view, the applied bias lowers the Fermi level of the metal below the Fermi level of the semiconductor. The $E_c$ and $E_v$ of the semiconductor also bend down following the principals of MS contact. The majority carriers for n-type semiconductors electrons are trapped on the interface between oxides-semiconductor shown on figure 3 (a). From the block charge diagram view, there are some positive charges accumulates on the metal gate because of the positive bias, the negatively excess electrons in the semiconductors are attracted toward the oxide-semiconductor interfaces shown in figure 3(b).

The second type of biasing region is depletion, where the concentration of the majority carriers has been depleted. This happens for n-type semiconductor when $V_G < 0$ (small). From the band diagram view, the applied bias raises the Fermi level of the metal higher than the Fermi level of the semiconductor. The negative slope bending (up direction bending) occurs for the semiconductor. The donors (electrons) are moving to the opposite direction which is moving to the right in figure 4 (a). The concentrations of the donors have been decreasing, and this is so-called depletion. From the block charge diagram view, the applied negative bias repels the electrons on the semiconductors away from the MOS interfaces. Therefore, the electrons are on the surface of the semiconductor, so in figure 4 (b) the widths of block charge are wider than figure 3 (b). Also, in this case, the electron concentrations of the semiconductor are less than the background doping concentration $N_D$.

Figure 3 Accumulation of n-type MOS devices (a) band diagram (b) block charge diagram.

Figure 4 Depletion of n-type MOS devices (a) band diagram (b) block charge diagram.
The third type of biasing region inversion happens if the biasing voltages keep increasing from the depletion region. For example, for n-type semiconductor, if the $V_G < 0$ (big) is applying. The inversion biasing region is where the Fermi level of the semiconductor start cross out from above the $E_i$ to below the $E_i$. The fact is emphasized by the red bubble in figure 5 (a). In the band diagram, the energy bands of semiconductor are bending more and more higher. The holes concentration at the surface increase as the concentration of the electrons decrease. At a threshold voltage ($V_T$), the surface region changes from n-type to p-type as $E_F$ of the semiconductor cross the $E_i$. Therefore, the figure 5 represents the band diagram and block charge diagram for inversion biasing when the applied bias equals to the threshold voltage, $V_G = V_T$. The figure 6 represents the both diagrams for inversion biasing when the applied bias is larger than the threshold voltage, $V_G > V_T$. In the block charge diagram, since the applied bias is large enough the holes attracted to the interface piled up in figure 6 (b), and the ionized holes are on the surface as in figure 5 (b) and figure 6 (b).

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C-V Characteristic Curve

The capacitance of the MOS-C devices behave as the function of applied voltage $V_G$. There are two limits: low frequency limit and high frequency limit. The behavior of both limits are shown in the Figure 7 for MOS-C device with n-type semiconductors. Their behaviors differ at inversion and inversion to transition regions but they converge at depletion, flat band and accumulation regions.
Conclusion

In summary, different types of biasing region depend on the biasing voltage applying to the MOS-C devices. Also, different doping of the n-type semiconductor and p-type semiconductor affects the biasing regions. The table 1 below shows the situation of how the MOS-C devices would be when specific VG is applying.

<table>
<thead>
<tr>
<th>Type / Applied Bias</th>
<th>VG=0</th>
<th>V_{T}&gt;VG&gt;0 (small)</th>
<th>VG&gt;V_{T} (Big)</th>
<th>V_{T}&lt;VG&lt;0 (small)</th>
<th>VG&lt;V_{T} (Big)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-type Semiconductor</td>
<td>Flat Band</td>
<td>Accumulation</td>
<td>Accumulation</td>
<td>Depletion</td>
<td>Inversion</td>
</tr>
<tr>
<td>p-type Semiconductor</td>
<td>Flat Band</td>
<td>Depletion</td>
<td>Inversion</td>
<td>Accumulation</td>
<td>Accumulation</td>
</tr>
</tbody>
</table>

Questions

(1) Use a line plot to show the magnitude of VG ranges corresponding to accumulation, depletion, and inversion in ideal n-type and p-type MOS devices. Please include the marking of V_{T}.

(2) What is the biasing region of the point a in the figure 8 below?

(3) What is the biasing region of the point b in the figure 8 below?

(4) What is the biasing region of the point c in the figure 8 below?

Figure 7 Capacitance verses voltage of MOS-C device for n-type semiconductor.
Figure 8. C-V curve of a MOS device (n-type semiconductor) for question 2, 3, and 4.

Answers

(1)

(2) Depletion

(3) Flat band

(4) Accumulation
References


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