9.3: Single Chip Oscillators and Frequency Generators

The generation of signals is a basic requirement for a wide variety of applications, thus a number of manufacturers produce a selection of single IC oscillators and frequency generators. Some of these tend to work in the range below 1 MHz and usually require some form of external resistor/capacitor network to set the operating frequency. Other, highly specialized circuits for targeted applications are also available. In this section we shall examine a few of the ICs that are generically referred to as clock generators, voltage-controlled oscillators, phase-locked loops and timers.

Square Wave/Clock Generator

The need for stable, low cost, easy-to-use integrated circuits to generate square waves for clocking needs is widespread. Several companies manufacture such devices. One example is the LTC6900 from Linear Technology. A description sheet with a basic programming formula is shown in Figure 9.26.
The LTC6900 is a 5 volt low power circuit available in an SOT-23 (5 pin) package. It operates from 1 kHz to 20 MHz. The output frequency is programmable via a single resistor and the connection to its divider pin (labeled DIV). The frequency of the master oscillator is given by the equation

\[ f_o = 10 \text{ MHz} \frac{20 \text{ k}}{R_{\text{set}}} \] \tag{9.33}

\(R_{\text{set}}\) is connected from the power supply pin to the SET pin. Acceptable values range between 10 kΩ and 2 MΩ. If the DIV pin is grounded, the output frequency will be as calculated. If the DIV pin is left unconnected, the output frequency will be divided by 10 and if the DIV pin is connected to +5 volts, the output frequency will be reduced by a factor of 100. This is summarized graphically in Figure 9.27.

Example 9.7

Using the LTC6900, design a 10 kHz square wave oscillator.

10 kHz is well within the range of this IC. To achieve this comfortably, we will need a divide-by-100 setting based on the graph of Figure 9.27. This will require us to tie the DIV pin to +5 volts. The value of \(R_{\text{set}}\) can be approximated from the graph or computed directly.

\[ f_{\text{osc}} = 10 \text{ MHz} \frac{20 \text{ k}}{N \times R_{\text{set}}} \]

\[ R_{\text{set}} = 10 \text{ MHz} \frac{20 \text{ k}}{100 \times 100 \text{ kHz}} \]

\[ R_{\text{set}} = 200 \text{ k} \]

Voltage-Controlled Oscillator

A voltage-controlled oscillator (usually abbreviated as VCO) does not produce a fixed output frequency. As its name suggests, the output frequency of a VCO is dependent on a control voltage. There is a fixed relationship between the control voltage and the output frequency. Theoretically, just about any oscillator can be turned into a VCO. For example, if a resistor is used as part of the tuning circuit, it could be replaced with some form of voltage-controlled resistor, such
as an FET or a light-dependent resistor/lamp combination. By doing this, an external potential can be used to set the frequency of oscillation. This is very useful if the frequency needs to be changed quickly or accurately swept through some range.

A classic example of the usefulness of a VCO is shown in Figure 9.28. This is a simplified schematic of an analog monophonic musical keyboard synthesizer. The keys on the synthesizer are little more than switches. These switches tap potentials off a voltage divider. As the musician plays up the keyboard, the switches engage higher and higher potentials. These levels are used to control a very accurate VCO. The higher the control voltage, the higher the output frequency or pitch will be.

![Figure 9.28 Simplified music synthesizer using VCO](https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Map%3A_Operational_Amplifiers_and_Linear_Integrators%2FChapter_9_Oscillators_and_Sweep_Sources/Section_9.6_Voltage_Controlled_Oscillators/)

VCOs can be used for a number of other applications, including swept frequency spectrum analyzers, frequency modulation and demodulation, and control systems. It is also an integral part of the phase-locked loop, as we will see later in this chapter.

An example of a VCO is the LTC6990. It is part of Linear Technology’s TimerBlox series of timer/counter/clock ICs. The series includes clock sources that operate in excess of 100 MHz and timers that switch at multi-hour rates. The LTC6990 operates in the range of just under 500 Hz to 2 MHz. While it can be used for fixed frequency applications, it also makes for a flexible VCO. An overview is shown in Figure 9.29.

![Figure 9.29 LTC6990 VCO](https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Map%3A_Operational_Amplifiers_and_Linear_Integrators%2FChapter_9_Oscillators_and_Sweep_Sources/Section_9.6_Voltage_Controlled_Oscillators/)
Like the LTC6900, the LTC6990 is programmed with as little as one resistor and has a frequency divider option. Unlike its brother, the divider capabilities are much more broad, spanning eight power-of-two settings versus just three decade settings. A basic fixed frequency oscillator is shown at the bottom left of Figure 9.29 where the master oscillation frequency is controlled by \( (R_{\text{set}}) \). Standard VCO operation is shown at the bottom right. The LTC6990 also has the option of a high impedance output state, making a total of 16 divider/output possibilities. This set up is programmed typically through the use of two external resistors. The programming table is reproduced in Figure 9.30.

<table>
<thead>
<tr>
<th>DIVCODE</th>
<th>( n )</th>
<th>( R_{\text{set}} )</th>
<th>Recommended ( R_1 )</th>
<th>( R_2 )</th>
<th>( V_{\text{DIV}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7</td>
<td>62 Ohm to 160kΩ</td>
<td>Open</td>
<td>Short</td>
<td>( 0 )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
<td>31.25kΩ to 50kΩ</td>
<td>6765</td>
<td>1022</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>4</td>
<td>15.625kΩ to 25kΩ</td>
<td>6765</td>
<td>1022</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>8</td>
<td>7.8125kΩ to 12.5kΩ</td>
<td>10800</td>
<td>208</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>16</td>
<td>3.90625kΩ to 6.25kΩ</td>
<td>10800</td>
<td>302</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>32</td>
<td>1.953125kΩ to 3.125kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>64</td>
<td>0.9765625kΩ to 1.5625kΩ</td>
<td>10800</td>
<td>1207</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>128</td>
<td>6.25kΩ to 10kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>64</td>
<td>0.9765625kΩ to 1.5625kΩ</td>
<td>10800</td>
<td>1207</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>128</td>
<td>6.25kΩ to 10kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>32</td>
<td>1.953125kΩ to 3.125kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>16</td>
<td>3.90625kΩ to 6.25kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>8</td>
<td>7.8125kΩ to 12.5kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>4</td>
<td>15.625kΩ to 25kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>2</td>
<td>31.25kΩ to 50kΩ</td>
<td>10800</td>
<td>603</td>
</tr>
<tr>
<td>15</td>
<td>0</td>
<td>62 Ohm to 160kΩ</td>
<td>Short</td>
<td>Short</td>
<td>( 0 )</td>
</tr>
</tbody>
</table>

The output state depends on the combination of the Output Enable pin (OE) and the Hi-Z logic. When OE is high, the output will be active. If OE is low and Hi-Z is low, then the output will be held low. Finally, if OE is low and Hi-Z is high, then the output will go to a high impedance state.

The voltage present at the DIVCODE pin sets the frequency divider and the impedance mode. This voltage is interpreted by an internal 4 bit analog-to-digital converter (AD converters are the topic of Chapter Twelve). While it is possible to feed this pin with some external source, the more practical method is to simply create a voltage divider with a pair of 1% tolerance resistors; one tied from the power supply to the DIVCODE pin, and the second connected from DIVCODE to ground.

The master oscillator of the LTC6990 is controlled by the current at the SET pin. Internally, the voltage at this pin is maintained at 1 volt, therefore the frequency can be set by a single resistor, \( (R_{\text{set}}) \), connected from this pin to ground. It can then be divided down to lower frequency. This is essentially the same situation we found with the LTC6900. A 20 μA current (i.e., 50 kΩ) will produce the top rate of 1 MHz. Lower currents (higher resistances) will produce proportionately lower frequencies.

The DIVCODE value will divide this base frequency down further by powers of two. We can express this relation with the following formula,

\[ f_{\text{osc}} = 1 \text{ MHz} \times \frac{50 \text{ k} \Omega}{N_{\text{DIV}} \times R_{\text{set}}} \]

where \( (N_{\text{DIV}}) \) is found from the table in Figure 9.30

The design process starts by identifying the appropriate frequency range. It is best if the desired oscillation frequency is not located at the extremes of any given range. Once a range is determined, the corresponding value for \( (N_{\text{DIV}}) \) is found, and along with it, the required divider resistor values, \( (R_{\text{1}}) \) and \( (R_{\text{2}}) \). From there it is a simple matter to solve
Equation \ref{9.34} in terms of \(R_{\text{set}}\).

Example 9.8

An LTC6990 is connected as shown in Figure 9.31. It is being used as a light-to-frequency converter. That is, the output frequency will be controlled by the amount of light hitting a sensor. The sensor is a CdS (Cadmium Sulfide) cell that is connected in the position of \(R_{\text{set}}\). Under low light conditions the cell will produce a high resistance and as the light level increases the resistance drops. Assuming that the cell varies from 500 k down to 60 k, determine the range of output frequencies. First, determine the DIVCODE value. This can be found by computing the voltage divider ratio of \(R_{\text{1}}\) and \(R_{\text{2}}\), but in this circuit recommended values have been used from the DIVCODE table. By observation, \(N_{\text{DIV}}\text{=}16\).

Next, we calculate the limit frequencies.

\[
\text{f}_{\text{osc}} = 1\text{MHz} \frac{50 \text{k}}{N_{\text{DIV}} R_{\text{set}}} \\
\text{f}_{\text{osc}} = 1\text{MHz} \frac{50\text{k}}{16 \times 500 \text{k}} \\
\text{f}_{\text{osc}} = 6.25 \text{kHz} \\
\text{f}_{\text{osc}} = 1\text{MHz} \frac{50 \text{k}}{N_{\text{DIV}} R_{\text{set}}} \\
\text{f}_{\text{osc}} = 1\text{MHz} \frac{50\text{k}}{16 \times 60 \text{k}}
\]
\[ f_{osc} = 52.08 \text{ kHz} \]

Note that as light levels increase, frequency increases in proportion.

When used in VCO mode, the most important element to remember is that the master oscillator frequency is set by the current coming out of the SET pin, \( I_{set} \), as expressed by the following formula
\[ f_o = 1 \text{ MHz} \times 50 \text{ k} \frac{I_{set}}{V_{set}} \]

\( V_{set} \) is kept to 1 volt internally so this reduces to
\[ f_o = 1 \text{ MHz} \times 50 \text{ k} \times I_{set} \tag{9.35} \]

\( f_{osc} \) is then divided down by \( N_{DIV} \). The final oscillation frequency may be expressed as
\[ f_{osc} = 1 \text{ MHz} \times 50 \text{ k} \frac{I_{set}}{N_{DIV}} \tag{9.36} \]

Note that \( I_{set} \) is exiting the chip. Further, note the frequency of oscillation and \( I_{set} \) are directly proportional. Also, keep in mind that the \( I_{set} \) variation, and hence, the frequency variation, should be kept to 16:1 for best performance, where the maximum value of \( I_{set} \) is 20 \( \mu \text{A} \). A simple method for obtaining voltage control is shown in Figure 9.29. There are some potential issues here. First, the range of voltage from the control circuit may not be able to achieve the desired frequency with that circuit. Second, note that higher control voltages will produce lower output frequencies, that is, an inverse relation. This can be an issue in some applications. Consequently, we shall examine a more generic method of controlling the circuit through the use of an external op amp for scaling and offsetting.

The circuit of Figure 9.32 presents a method of mapping the existing control voltage onto the LTC6990 or any similar VCO. In this circuit a simple summing amplifier is used for scaling and offsetting. The control voltage, \( V_C \), is scaled by one channel of the weighted summer. This signal is offset by a DC voltage, \( V_{offset} \), fed through another channel. The voltage at the output of the op amp is used to sink current from the VCO via the control resistor, \( R_C \).

Recall that the SET pin of the IC produces 1 volt internally and it is the exiting current, \( I_{set} \), that sets the master oscillator frequency, as expressed in Equation \ref{9.35}. Obviously, the op amp output voltage must be less than 1 volt in order for the op amp to sink current (i.e., in order for \( I_{set} \) to be exiting the LTC6990). The voltage difference between the op amp’s output and the 1 volt at the SET pin drops across \( R_C \) and this is what creates \( I_{set} \). Note that as the control voltage grows more positive at the op amp’s input, its output, and hence \( I_{set} \), also increases. Thus, frequency increases as control voltage increases.

Example 9.9

Using Figure 9.32 as a guide, design a VCO circuit that will produce output frequencies from 20 kHz through 50 kHz
when driven by control voltages from 6 to 8 volts (i.e., 6 volts will produce 20 kHz, 7 volts will produce 35 kHz, 8 volts will produce 50 kHz, etc.)

First, note that the frequency range is 2.5:1. As the LTC6990 can always cover any 8:1 span (as high as 16:1) and the maximum frequency of 50 kHz is well below the LTC6990's maximum, we know this IC is a good candidate for the design. We now need to determine the divider resistor values. Consulting Figure 9.30 shows that we can achieve this range using an \(N_{(\text{DIV})}\) of 4, 8 or 16. Choosing the middle value, and assuming we don't care about Hi-Z state, we arrive at DIVCODE=3 with \(R_{(1)}=1\, \text{M\Omega}\) and \(R_{(2)}=280\, \text{k\Omega}\).

Our frequency range is 2.5:1 which means that our \(I_{(\text{set})}\) range must also be 2.5:1. For convenience, choose the op amp's output to be 0 volts for the minimum frequency. This will yield 1 volt across \(R_{(C)}\) and occurs when the control voltage into the op amp is at its 6 volt minimum. When the control voltage is at its maximum of 8 volts we'll need 2.5 volts across \(R_{(C)}\) (i.e., 2.5 times the prior \(I_{(\text{set})}\)). This means that the op amp's output must go to -1.5 volts. Note that a 2 volt change in the input control voltage will produce a 1.5 volt change at the op amp's output. Thus, the gain of this channel is -0.75. If we choose \(R_{(f)}=100\, \text{k\Omega}\) then \(R_{(b)}=75\, \text{k\Omega}\).

At this point we need to add an offset. With only the gain scaling, the 6 volt \(V_{(C)}\) produces -0.75 times 6, or -4.5 volts, and a \(V_{(C)}\) of 8 volts similarly produces -6 volts. Consequently, we need to add a +4.5 volt offset to the output. If we tie \(V_{(\text{offset})}\) to the op amp's -15 volt power rail then we will need a gain of 4.5/(-15), or -0.3. With an \(R_{(f)}\) of 100 k\Omega, \(R_{(a)}\) must be 333.3 k\Omega (the nearest 1% standard value is 332 k\Omega).

Finally, to determine \(R_{(C)}\), refer to Equation \ref{9.36} and solve for \(I_{(\text{set})}\)

\[
I_{(\text{set})} = \frac{f_{\text{osc}} \times N_{(\text{DIV})}}{1 \, \text{MHz} \times 50 \, \text{k}}
\]

Using the minimum fosc of 20 kHz yields

\[
I_{(\text{set})} = \frac{20 \, \text{kHz} \times 8}{1 \, \text{MHz} \times 50 \, \text{k}}
\]

\[
I_{(\text{set})} = 3.2 \, \mu\text{amps}
\]

This occurs with 1 volt across \(R_{(C)}\). Therefore \(R_{(C)} = 312.5\, \text{k\Omega}\). Crosschecking, when \(V_{(C)} = 8\, \text{V}\), we see 2.5 volts across \(R_{(C)}\) for a current of 8 \(\mu\text{A}\). Inserting this into Equation \ref{9.36} yields 50 kHz, our desired maximum frequency.

In closing, note that the way in which the frequency sweeps depends on the wave shape of \(V_{(c)}\). If a sinusoid is used, the output frequency will vary smoothly between the stated limits. On the other hand, if the wave shape for \(V_{(c)}\) is a ramp, the output frequency will start at one extreme and then move smoothly to the other limit as the \(V_{(c)}\) ramp continues. When the ramp resets itself, the output frequency will jump back to its starting point. An example of this is shown in Figure 9.33. Finally, if the control wave shape is a square, the output frequency will abruptly jump from the minimum to the maximum frequency and back. This effect is shown in Figure 9.34, and can be used to generate FSK (frequency shift key) signals. FSK is used in the communications industry to transmit binary information.
Phase-Locked Loop

One step up from the VCO is the Phase-Locked Loop, or PLL. The PLL is a selfcorrecting circuit; it can lock onto an input frequency and adjust to track changes in the input. PLLs are used in modems, for FSK systems, frequency synthesis, tone decoders, FM signal demodulation, and other applications. A block diagram of a basic PLL is shown in Figure 9.35.

In essence, the PLL uses feedback in order to lock an oscillator to the phase and frequency of an incoming signal. It consists of three major parts; a phase comparator, a loop filter (typically, a lag network of some form), and a VCO. An amplifier may also exist within the loop. The phase comparator is driven by the input signal and the output of the VCO. It produces an error signal that is proportional to the phase difference between its inputs. This error signal is then filtered in order to remove spurious high-frequency signals and noise. The resulting error signal is used as the control voltage for the VCO, and as such, sets the VCO's output frequency. As long as the error signal is not too great, the loop will be selfstabilizing. In other words, the error signal will eventually drive the VCO to be in perfect frequency and phase synchronization with the input signal. When this happens, the PLL is said to be in lock with the input. The range of frequencies over which the PLL can stay in lock as the input signal changes is called the lock range. Normally, the lock range is symmetrical about the VCO's free-running, or center, frequency. The deviation from the center frequency out to the edge of the lock range is called the tracking range, and is therefore one-half of the lock range. This is illustrated in Figure 9.36.

Although a PLL may be able to track changes throughout the lock range, it may not be able to initially acquire sync with frequencies at the range limits. A somewhat narrower band of frequencies, called the capture range, indicates frequencies that the PLL will always be able to lock onto. Again, the capture range is usually symmetrical about \( f_{\text{ol}} \). The deviation on either side of \( f_{\text{ol}} \) is referred to as the pull-in range. For a PLL to function properly, the input
frequency must first be within the capture range. Once the PLL has locked onto the signal, the input frequency may vary throughout the larger lock range. The VCO center frequency is usually set by an external resistor or capacitor. The loop filter may also require external components. Depending on the application, the desired output signal from the PLL may be either the VCO's output, or the control voltage for the VCO.

One way to transmit binary signals is via FSK. This may be used to allow two computers to exchange data over telephone lines. Due to limited bandwidth, it is not practical to directly transmit the digital information in its normal pulse-type form. Instead, logic high and low can be represented by distinct frequencies. A square wave, for example, would be represented as an alternating set of two tones. FSK is very easy to generate. All you need to do is drive a VCO with the desired logic signal. To recover the data, the reception circuit needs to create a high or low level, depending on which tone is received. A PLL may be used for this purpose. The output signal will be the error signal that drives the VCO. The logic behind the circuit operation is deceptively simple. If the PLL is in lock, the output frequency of its VCO must be the same as the input signal. Remembering that the incoming FSK signal is itself derived from a VCO, for the VCOs to be in lock, they must be driven with identical control signals. Therefore, the control signal that drives the PLL’s internal VCO must be the same as the control signal that originally generated the FSK signal. The PLL control signal can then be fed to a comparator in order to properly match the signal to the following logic circuitry.

Along the same lines as the FSK demodulator is the standard FM signal demodulator. Again, the operational logic is the same. In order for the PLL to remain in lock, its VCO control signal must be the same as the original modulating signal. In the case of typical radio broadcasts, the modulating signal is either voice or music. The output signal will need to be AC coupled and amplified further. The PLL serves as the intermediate frequency amplifier, limiter, and demodulator. The result is a very cost-effective system.

Another usage for the PLL is in frequency synthesis. From a single, accurate signal reference, a PLL may be used to derive a number of new frequencies. A block diagram is shown in Figure 9.37. The major change is in the addition of a programmable divider between the VCO and the phase comparator. The PLL can only remain in lock with the reference oscillator by producing the same frequency out of the divider. This means that the VCO must generate a frequency $N(\text{Hz})$ times higher than the reference oscillator. We can use the VCO output as desired. In order to change the output frequency, all that needs to be changed is the divider ratio. Normally, a highly accurate and stable reference, such as a quartz crystal oscillator, is used. In this way, the newly synthesized frequencies will also be very stable and accurate.

One example of an advanced digital PLL is the LTC6950. This device operates at up to 1.4 GHz and has five outputs. Each of the outputs has an independently programmable divider and VCO clock cycle delay. The input reference frequency is set between 2 MHz and 250 MHz. Due to the multiple outputs and syncing capabilities, this device can be used for large distributed systems that require precisely controlled multiple clocks. Indeed, one device can be used to control several other LTC6950s for very large systems. An example of this would be a system making use of several high-speed high-resolution analog-to-digital or digital-to-analog converters. The accuracy of these devices depends greatly on very accurate and stable clock sources. We will examine analog-to-digital-to-analog conversion in Chapter

https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Map%3A_Operational_Amplifiers_and_Linear_Integr...
Twelve.

555 Timer

The 555 timer is a versatile integrated circuit first introduced in the early 1970's by Signetics. It has remained a popular building block in a variety of applications ranging from simple square wave oscillators to burglar alarms to pulse-width modulators and beyond. In its most basic forms, the one-shot, or monostable, and the astable oscillator, the 555 requires only a handful of external components. Usually, only two capacitors and two resistors are needed for basic functions. The 555 is made by different manufacturers and in a few forms. The 556, for example, is a dual 555. The 555 can produce frequencies up to approximately 500 kHz. The output current is specified as 200 mA, although this entails fairly high internal voltage drops. A more reasonable expectation would be below 50 mA. The circuit may be powered from supplies as low as 5 volts and as high as 18 volts. This makes the 555 suitable for both TTL digital logic and typical op amp systems. Rise and fall times for the output square wave are typically 100 ns.

A block diagram of the 555 is shown in Figure 9.38. It is comprised of a pair of comparators tied to a string of three equal-valued resistors. Note that the upper, or Threshold, comparator sees approximately 2/3 of \(V_{cc}\) at its inverting input, assuming no external circuitry is tied to the Control pin. (If the Control pin is unused, a 10 nF capacitor should be placed between the pin and ground.) The lower, or Trigger, comparator sees approximately 1/3 of \(V_{cc}\) at its noninverting input. These two comparators feed a flip-flop, which in turn feeds the output circuitry and Discharge and Reset transistors. If the flip-flop output is low, the Discharge transistor will be off. Note that the output stage is inverting, so that when the flip-flop output is low, the circuit output is high. In contrast, if the input to the Reset transistor is low, this will inhibit the output signal. If Reset capabilities are not needed, the Reset pin should be tied to \(V_{cc}\).

Returning to the comparators, if the noninverting input of the Threshold comparator were to rise above 2/3 \(V_{cc}\), the comparator’s output would change state, triggering the flip-flop and producing a low out of the 555. Similarly, if the input to the inverting input of the Trigger comparator were to drop below 1/3 \(V_{cc}\), the comparator’s output would change, and ultimately, the 555 output would go high.

555 Monostable Operation

The basic monostable circuit is shown in Figure 9.39. In this form, the 555 will produce a single pulse of predetermined width when a negative going pulse is applied to the trigger input. Note that the three input components, \(\text{R}_{\text{in}}\),
\( (C_{in}) \) and \( (D) \) serve to limit and differentiate the applied pulse. In this way, a very narrow pulse will result which reduces the possibility of false triggers. To see how the circuit works, refer to the waveforms presented in Figure 9.40.

Assume that the output of the 555 is initially low. This implies that the Discharge transistor is on, shorting the timing capacitor \( (C) \). A narrow low pulse is applied to the input of the circuit. This will cause the Trigger comparator to change state, firing the flip-flop, which in turn will cause the output to go high and also turn off the Discharge transistor. At this point, \( (C) \) begins to charge toward \( (V_{cc}) \) through \( (R) \). When the capacitor voltage reaches \( 2/3 (V_{cc}) \), the Threshold comparator fires, setting the output low and turning on the Discharge transistor. This drains the timing capacitor, and the circuit is ready for the application of a new input pulse. Note that without the input waveshaping network, the trigger pulse must be narrower than the desired output pulse. The Equation for the output pulse width is

\[
T_{\text{out}} = 1.1 \, RC
\]

An interesting item to note is that the value of \( (V_{cc}) \) does not enter into the equation. This is because the comparators are always comparing the input signals to specific percentages of \( (V_{cc}) \) rather than to specific voltages.

**Example 9.10**

Determine values for the timing resistor and capacitor to produce a 100 μs output pulse from the 555.

A reasonable choice for \( (R) \) would be 10 kΩ.

\[
T_{\text{out}} = 1.1 \, RC
\]
\[ C = \frac{T_{\text{out}}}{1.1 \, R} \notag \]
\[ C = \frac{100 \mu s}{1.1 \times 10 \, k} \notag \]
\[ C = 9.09 \, \text{nF} \notag \]

The nearest standard value would be 10 nF, so a better choice for \( R \) might be 9.1 kΩ (also a standard value). This pair would yield the desired pulse width quite accurately.

### 555 Astable Operation

Figure 9.41 shows the basic astable, or free-running form, for a square wave generator. Note the similarities to the monostable circuit. The obvious difference is that the former trigger input is now tied into the resistor-capacitor timing network. In effect, the circuit will trigger itself continually. To see how the circuit works, refer to Figure 9.42 for the waveforms of interest.

Assume initially that the 555 output is in the high state. At this point, the Discharge transistor is off and capacitor C is charging toward Vcc through RA and RB. Eventually, the capacitor voltage will exceed 2/3 Vcc causing the Threshold comparator to trigger the flip-flop. This will turn on the Discharge transistor and make the 555 output go low. The Discharge transistor effectively places the upper end of RB at ground, removing RA and Vcc from consideration. C now discharges through RB toward 0. Eventually, the capacitor voltage will drop below 1/3 Vcc. This will fire the Trigger comparator, which will in turn place the circuit back to its initial state, and the cycle will repeat.

![Figure 9.41](https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Map%3A_Operational_Amplifiers_and_Linear_Integrators%2FSection_9.4%3A_555_Timer%2F9aa5b1f305f7d71e8b22643e8c4ac589.png)

**Figure 9.41**

555 astable connection
The frequency of oscillation clearly depends only on $C$, $R_A$, and $R_B$. The time periods are

\[ T_{\text{high}} = 0.69(R_A+R_B)C \notag \]
\[ T_{\text{low}} = 0.69 R_B C \notag \]

This results in a frequency of

\[ f = \frac{1.44}{R_A +2 R_B} \notag \]

The duty cycle is normally defined as the high time divided by the period. The 555 documentation often reverses this definition, but we will stick with the industry norm.

\[ \text{Duty Cycle} = \frac{R_A+R_B}{R_A+2 R_B} \notag \]

A quick examination of the duty cycle Equation shows that there is no reasonable combination of resistors that will yield 50% duty cycle, let alone anything smaller. There is a simple trick to solve this problem, though. All you need to do is place a diode in parallel with $R_B$ as illustrated in Figure 9.43. The diode will be forward biased during the high time period and will effectively short out $R_B$. During the low time period the diode will be reverse-biased, and $R_B$ will still be available for the discharge phase. If $R_A$ and $R_B$ are set to the same value, the end result will be 50% duty cycle. Of course, due to the non-ideal nature of the diode, this will not be perfect, so some adjustment of the resistor values may be in order. Further, note that if $(R_A)$ is also replaced with a potentiometer (and perhaps a series limiting resistor) a tunable square wave generator will result.

\[ \text{Example 9.11} \]

Determine component values for a 2 kHz square wave generator with an 80% duty cycle. First, note the period is the
reciprocal of the desired frequency, or 500 μs. For an 80% duty cycle, that yields

\[
T_{\text{high}} = \text{Duty Cycle} \times T \\
T_{\text{high}} = 0.8 \times 500 \mu s \\
T_{\text{high}} = 400 \mu s \\
T_{\text{low}} = T - T_{\text{high}} \\
T_{\text{low}} = 500 \mu s - 400 \mu s \\
T_{\text{low}} = 100 \mu s \\
\]

Choosing \((R_B = 10 \, k\Omega)\),

\[
T_{\text{low}} = 0.69 R_B C \\
C = \frac{T_{\text{low}}}{0.69 R_B} \\
C = \frac{100 \mu s}{0.69 \times 10 \, k\Omega} \\
C = 14.5 \, nF \\
T_{\text{high}} = 0.69(R_A+R_B)C \\
R_A = \frac{T_{\text{high}}}{0.69C} - R_B \\
R_A = \frac{400 \mu s}{0.69 \times 14.5 \, nF} - 10 \, k\Omega \\
R_A = 30 k\Omega \\
\]

**Summary**

Oscillators and frequency generators find use in a wide variety of applications. They may be realized from simple single op amp topologies or use more elaborate special purpose integrated circuits. Basic op amp oscillators are usually constrained to the frequency range below 1 MHz. Two sine wave oscillators that are based on op amps are the Wien bridge and phase shift types. Both oscillators rely on positive feedback in order to create their outputs. To maintain oscillation, the amplifier/feedback loop must conform to the Barkhausen criterion. This states that in order to maintain oscillation, the loop phase must be 0°, or an integer multiple of 360°. Also, the product of the positive feedback loss and the forward gain must be greater than unity to start oscillations and revert to unity to maintain oscillation. In order to make the gain fall back to unity, some form of gain limiting device, such as a diode or lamp, is included in the amplifier's negative feedback loop. The oscillation frequency is usually set by a simple resistor/capacitor network. As such, the circuits are relatively easy to tune. Their ultimate accuracy will depend on the tolerance of the tuning components and, to a lesser degree, on the characteristics of the op amp used.
Besides sine waves, other shapes such as triangles and squares may be produced. A simultaneous square/triangle generator may be formed from a ramp generator/comparator combination. Only two op amps are required to realize this design.

The voltage-controlled oscillator, or VCO, produces an output frequency that is dependent on an external control voltage. The free-running, or center, frequency is normally set via a resistor/capacitor combination. The control voltage may then be used to increase or decrease the frequency about the center point. The VCO is an integral part of the phase-locked loop, or PLL. The PLL has the ability to lock onto an incoming frequency. That is, its internal VCO frequency will match the incoming frequency. Should the incoming frequency change, the internal VCO frequency will change along with it. Two important parameters of the PLL are the capture range and the lock range. Capture range is the range of frequencies over which the PLL can acquire lock. Once lock is achieved, the PLL can maintain lock over a somewhat wider range of frequencies called the lock range. The PLL is in wide use in the electronics industry and is found in such applications as FM demodulation, FSK based communication systems, and frequency synthesis.

Timers can be used to generate rectangular waves of various duty cycles as well as single-shot pulses.

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**Review Questions**

1. How does positive feedback differ from negative feedback?
2. Define the Barkhausen criterion.
3. Explain the operation of the Wien bridge op amp oscillator.
4. Detail the operation of the phase shift op amp oscillator.
5. How might a square wave be generated from a sinusoidal or triangular source?
6. Give two ways to make the output frequency of a Wien bridge oscillator user-adjustable.
7. What factors contribute to the accuracy of a Wien bridge oscillator’s output frequency?
8. What is a VCO, and how does it differ from a fixed-frequency oscillator?
9. Draw a block diagram of a PLL and explain its basic operation.
10. What is the difference between capture range and lock range for a PLL?
11. Give at least two applications for a fixed-frequency oscillator or VCO.
12. Give at least two applications for the PLL.
13. Explain the difference between astable and monostable operation of a timer.

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**Problems**

**Analysis Problems**

Unless otherwise specified, all circuits use ±15 V power supplies.

1. Given the circuit of Figure 9.44, determine the frequency of oscillation if \( R_1 = 1.5 \, k\Omega \), \( R_2 = R_3 = R_4 = 3 \, k\Omega \), and \( C_1 = C_2 = 22 \, nF \).
2. Given the circuit of Figure 9.44, determine the frequency of oscillation if \( R_2 = 22 \, k\Omega \), \( R_1 = R_3 = R_4 = 11 \, k\Omega \), and \( C_1 = C_2 = 33 \, nF \).

3. Given the circuit of Figure 9.45, determine the maximum and minimum \( f_o \) if \( R_1 = 5.6 \, k\Omega \), \( R_2 = 12 \, k\Omega \), \( R_3 = R_4 = 1 \, k\Omega \), \( P_1 = P_2 = 10 \, k\Omega \), \( C_1 = C_2 = 39 \, nF \).

4. Given the circuit of Figure 9.46, determine \( f_o \) if \( R_4 = 2 \, k\Omega \), \( R_3 = 20 \, k\Omega \), \( R_2 = 200 \, k\Omega \), \( R_1 = 1.6 \, M\Omega \), \( C_1 = 30 \, nF \), \( C_2 = 3 \, nF \), \( C_3 = 300 \, pF \).

5. Given the circuit of Figure 9.46, determine \( f_o \) if \( R_1 = R_3 = R_4 = 3.3 \, k\Omega \), \( R_2 = 100 \, k\Omega \), \( C_1 = C_2 = C_3 = 86 \, nF \).

6. Given the circuit of Figure 9.47, determine \( f_o \) if \( R_1 = R_2 = 22 \, k\Omega \), \( R_3 = 33 \, k\Omega \), \( C = 3.3 \, nF \).

7. Using the circuit of Figure 9.48, determine the output voltage if \( R_{\text{set}} = 100 \, k\Omega \).
8. Using the circuit of Figure 9.49, determine the output voltage if \( R_{\text{set}} = 50 \, \text{k}\)Ω.

9. A temperature dependent resistor, or thermistor, is used in Figure 9.50. If the resistance varies between 20 \( \text{k}\)Ω and 200 \( \text{k}\)Ω through the temperature range of interest, determine the range of output frequencies.

10. For the circuit of 9.51, determine the range of output frequencies if \( V_C \) varies between 0 V and -1 V. \( R_C = 100 \, \text{k}\)Ω, \( R_1 = 1 \, \text{M}\)Ω, \( R_2 = 681 \, \text{k}\)Ω.

11. For the circuit of Problem 9.10, determine the output frequencies if \( V_C \) is a 100 Hz square wave at 0.5 volts peak.

12. Sketch the output waveform for Problem 9.11.
13. If a control voltage of 0.4 sin 2π60t is used for the circuit of Problem 9.10, find the resulting maximum and minimum output frequencies.

14. Given the circuit of Figure 9.52, determine the output frequency if \( V_C = 2 \) V, \( R_{VCO} = R_{set} = 100 \) kΩ, \( R_1 = 976 \) kΩ and \( R_2 = 102 \) kΩ.

15. Given the circuit of Figure 9.47, determine \( f_0 \) if \( R_1 = R_2 = 22 \) kΩ, \( R_3 = 33 \) kΩ, and \( C = 3.3 \) nF.

16. Determine the output frequency range in Figure 9.53 if \( V_C \) varies from 0 to 2 volts, \( R_f = 200 \) kΩ, \( R_i = 100 \) kΩ, \( R_C = 500 \) kΩ, \( R_1 = 976 \) kΩ and \( R_2 = 182 \) kΩ.

17. Determine the output frequency range in Figure 9.54 if \( V_b \) varies from 0 to 2 volts, \( V_a = 1 \) volt, \( R_f = 200 \) kΩ, \( R_a = 100 \) kΩ, \( R_b = 200 \) kΩ, \( R_C = 390 \) kΩ, \( R_1 = 182 \) kΩ and \( R_2 = 976 \) kΩ.

**Design Problems**

18. For the circuit of Figure 9.44, determine values for \( C_1 \) and \( C_2 \) if \( R_1 = 6.8 \) kΩ, \( R_2 = R_3 = R_4 = 15 \) kΩ, and \( f_0 = 30 \) kHz.

19. For the circuit of Figure 9.44, determine values for \( R_3 \) and \( R_4 \) if \( R_1 = 2.2 \) kΩ, \( R_2 = 4.7 \) kΩ, \( C_1 = C_2 = 47 \) nF, and \( f_0 = 400 \) Hz.

20. For the circuit of Figure 9.44, determine values for \( R_2, C_1 \) and \( C_2 \) if \( R_1 = 7.2 \) kΩ, \( R_3 = R_4 = 3.9 \) kΩ, and \( f_0 = 19 \) kHz.

21. Determine the values required for \( R_3, R_4, P_1 \), and \( P_2 \) in Figure 9.45 if \( C_1 = C_2 = 98 \) nF, \( f_0 = 5.6 \) kHz.
kΩ, R₂ = 12 kΩ, f_{o.min} = 2 kHz, and f_{o.max} = 20 kHz.

22. Repeat Problem 21 for f_{o.min} = 10 kHz and f_{o.max} = 30 kHz.

23. Redesign the circuit of Problem 1 so that exact gain resistors are not needed. Use Figure 9.6 as a model.

24. Redesign the circuit of Problem 3 so that clipping does not occur. Use Figure 9.6 as a model.

25. Determine new values for the capacitors of Problem 4 if fo is changed to 10 kHz.

26. Given the circuit of Figure 9.46, determine values for the capacitors if R_1 = R_3 = R_4 = 3.3 kΩ, \( R_2 = 100 \) kΩ, and f_o = 7.6 kHz.

27. Given the circuit of Figure 9.46, determine values for the resistors if the capacitors all equal 1100 pF and fo = 15 kHz.

28. Determine the capacitor and resistor values for the circuit of Figure 9.46 if \( R_2 = 56 kΩ \) and f_o = 1 kHz.

29. Find C in Figure 9.47 if f_o = 5 kHz, R_1 = R_3 = 39 kΩ, R_2 = 18 kΩ.

30. Determine the resistor values in Figure 9.47 if f_o = 20 kHz and \( C = 22 nF \). Set \( R_1 = R_2 \) and \( R_2 = R_3/2 \). Sketch the output waveforms as well.

31. Determine the required ratio for \( R_2/R_3 \) to set the triangle wave output to 5 V peak in Figure 9.47.

32. Using the circuit of Figure 9.48, find \( R_{set} \) for an output of 100 kHz.

33. Determine the value for \( R_{set} \) in Figure 9.49 to set the frequency to 50 kHz.

34. Design a square wave generator that is adjustable from 5 kHz to 20 kHz.

35. For the circuit of Figure 9.52, determine the component values such that a frequency of 250 kHz is produced when \( V_C = 0 \) volts and 125 kHz when \( V_C = 1 \) volt.

36. Design a \( V_{CO} \) circuit and determine the component values such that a frequency of 250 kHz is produced when \( V_C = 1 \) volt and 125 kHz when \( V_C = 0 \) volts.

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**Challenge Problems**

37. Using Figure 9.9 as a guide, design a sine wave oscillator that will operate from 2 Hz to 20 kHz, in decade ranges.

38. Design a 10 kHz TTL-compatible square wave oscillator using a Wien bridge oscillator and a 311 comparator.

39. Using a triangle or sine wave oscillator and a comparator, design a variable duty cycle pulse generator. Hint: Consider varying the comparator reference.

40. Using a function synthesizer (Chapter Seven) and the oscillator of Figure 9.47, outline a simple laboratory frequency generator with sine, triangle, and square wave outputs.

41. For the preceding problem, outline how amplitude and DC offset controls could be implemented as well.

42. Generate a square wave that smoothly increases from 50 kHz to 300 kHz and back at a rate 100 times each second.

43. Assume that the output of the left-most op amp of Figure 9.47 drives Vb of Figure 9.54. Further, assume that a positive DC voltage equal to the peak value of \( V_b \) is used to drive \( V_a \). Also, \( R_a = R_b = R_f \). Assuming the frequency produced by Figure 9.47 is considerably lower than that of Figure 9.54, describe the output waveform of Figure 9.54.
Computer Simulation Problems

44. Perform a simulation of the circuit of Problem 1. Perform a frequency domain analysis of the positive feedback loop's gain and phase, and verify that the Barkhausen Criterion is met.

45. Perform a simulation for the circuit of Problem 4. Perform a frequency domain analysis of the positive feedback loop's gain and phase, and verify that the Barkhausen Criterion is met.

46. Perform a time-domain simulation analysis for the circuit of Problem 6. Make sure that you check both outputs (a simultaneous plot would be best).